NASA CASE NO. NPO-16,784-1CU

PRINT FIG. 3

NOTICE

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NRO-JPL

(NASA-Case-NPO-16784-1) CROSS-CONTACT CHAIN Patent Application (NASA) 16 p CSCL 09A

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AWARDS ABSTRACT

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JPL No. 16784
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CROSS-CONTACT CHAIN

The object of the disclosure is to provide an economical system for testing the reliability of a batch of integrated circuits while they are still on a large wafer.

Test circuits 30 (Fig. 1) are formed on the same wafer as the integrated circuits 12. Each test circuit has upper and lower layers 14, 16 (Fig. 2) in contact at interfaces 24. A high resistance between opposite ends 25, 27 of the interface would indicate poor circuits on the wafer. The test circuit has several conductive strips 40 - 42, etc. (Fig. 5), alternating between the upper and lower layers and connected at interfaces 51 - 53, etc., to form a contact chain. A current source 70 (Fig. 4) passes current between tabs T_2, T_{23} at opposite ends of the contact chain, so the current is flowing through each interface 51-60 along the chain. During such current flow, voltmeter VM takes voltage measurements across pairs of tabs such as T_1 and T_4 that are connected to opposite ends of an interface 51, to measure the resistance across the interface. Such measurements are taken for eleven sets of tabs T_1, T_4; T_3, T_6; and so forth up to tabs T_{21}, T_{24}. The voltage measurements indicate interface resistance, or conductance. The conductance measurements can be plotted on a normal probability graph (Fig. 8), with each point such as 106 having an ordinate R equal to the conductance of a measurement. Measurements of progressively lower conductance are located at progressively greater abscissa values A with respect to a point 104 of lowest abscissa. An imaginary straight line 110 closest to the points, passes through a conductance level too low for reliable operation (e.g., 1 mho) at a probability such as 5N = 99.999%. This indicates that one in 100,000 interfaces will be defective.

One point of novelty is providing multiple pairs of tabs along a contact chain, with two tabs at the ends of the chain used to pass current through the chain, and the pairs of tabs used to take voltage measurements to determine interface conductance. Another point of novelty is the plotting of a large number of conductances on a normal probability graph to determine the probability of a failure.

JPL Case No. 16784
~~NASA Case No.~~ NPO-16784-1-CU

CROSS-CONTACT CHAIN

ORIGIN OF THE INVENTION

The invention described herein was made in the performance of work under a NASA contract, and is subject to the provisions of Public Law 96-517 (35 USC 202) in which the Contractor has elected not to retain title.

BACKGROUND OF THE INVENTION

A wafer containing numerous integrated circuits, will generally include at least two conductive (or semi-conductive) layers, one lying above the other and separated by an insulator, and with the layers interconnected at numerous interfaces. High resistance at such interfaces is a major source of defects. One way to measure interface resistance is to form one or more contact chains on the wafer, at locations adjacent to some or all of the integrated circuits. Each contact chain has many conductive segments formed in each layer, and the conductive segments are connected in series by interfaces between the layers. A pair of tabs is provided at opposite ends of a chain containing the many interfaces in series, and the resistance between the tabs is measured. While this can indicate the existence of a catastrophic failure (a very high resistance interface), it does not provide information as to the resistence at each of the many interfaces.

The detection of the resistance at each of several interfaces can be made by providing four pairs of terminals or tabs for each interface. Current can pass between a first pair of tabs while the voltage is

measured across the other pair of tabs, to determine the resistance across that interface. However, the need for a large number of tabs such as 44 tabs for testing 11 interfaces, gives rise to the problem that there may not be sufficient room on the wafer for so many tabs. A system which facilitated the measurement of resistance across each of numerous interfaces while minimizing the number of tabs required, and simplified the test instrument requirements, would facilitate the testing of integrated circuits. The utilization of such interface measurements to predict the yield of integrated circuits, would be of further value.

SUMMARY OF THE INVENTION

In accordance with one embodiment of the present invention, a system is provided for facilitating the testing of integrated circuits, and in particular the interfaces between different conducting (or semi-conducting) layers of a circuit. A contact chain can be established beside an integrated circuit, the chain including a plurality of conductive segments formed in the two layers, and interfaces between the two layers for conducting segments in alternate layers in series. A first and last conductive tab is connected to the end of the chain to enable a current to be passed along the chain through its interfaces. A plurality of pairs of voltage tabs are provided which connect to the two different layers at each interface along the chain, to enable a voltage measurement to be made across a corresponding interface. While a current is passing along the length of the chain, the instrument makes voltage measurements across the pairs of voltage tabs, to thereby measure the resistance or conductances across each of the interfaces.

The conductances measured across the numerous interfaces can be plotted on a normal probability

graph, with each point on the graph having an ordinate equal to the conductance across an interface, and with points of progressively lower conductance having abscissas progressively further from a minimum abscissa value of the graph. A straight line passing approximately through the points, can be extended to indicate the probability that one of the interfaces will be below a level required for operation of a circuit containing the interface. This enables a determination of the probability of a catastrophic failure of an integrated circuit containing the interfaces.

The novel features of the invention are set forth with particularity in the appended claims. The invention will be best understood from the following description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a simplified plan view of a workpiece constructed in accordance with the present invention.

Fig. 2 is a sectional side view of an interface in the workpiece of Fig. 1.

Fig. 3 is a plan view of a portion of a test circuit of the workpiece of Fig. 1, with the lower layer highlighted by cross hatch-like lines.

Fig. 4 is a plan view similar to that of Fig. 3, but showing additional portions of the test circuit.

Fig. 5 is a partial perspective view of the test circuit portion of Fig. 3.

Fig. 6 is an enlarged view of a portion of the circuit of Fig. 5.

Fig. 7 is a diagrammatic view of a test instrument useful with the test circuit of Fig. 3.

Fig. 8 is a normal probability graph of conductances versus probability, that can be

constructed from data obtained with the test instrument of Fig. 7.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 illustrates a workpiece 10 in the form of a wafer or substrate which contains many integrated circuits 12. Each integrated circuit includes a pair of conductive (possibly semi-conductive) layers that are separated with one below the other, but with the layers in contact at interfaces.

Fig. 2 illustrates a portion of such an arrangement, wherein a first level (Schottky) metal layer ~~14~~ 16 lies ~~above~~ below a second level metal layer ~~18~~ 14, the two layers being isolated by an insulator 18. The insulator 18 has a hole 20 ("Vias") which is plated by a conductor 22 such as a portion of the upper layer 14. The conductor 22 makes contact with the lower layer 16 at an interface 24. The resistance at the interface 24 is preferably as low as possible, but may be unexpectedly high due to oxides and residues. It is such high resistance, or low conductance, at an interface, which is a major source of faults in the integrated circuits. The interface resistance can be measured by passing a current between opposite ends 25, 27 of the interface, and measuring the voltage between the interface opposite ends.

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In order to determine the condition of the interfaces, test circuits 30 (Fig. 1) can be formed on the same workpiece 10 which contains the integrated circuits. The test circuit includes regions of the upper and lower layers 14, 16 and interfaces 24 between them. The test circuit also has conductive terminals or tabs on the surface of the workpiece, where test instruments can make contact with the tabs to measure resistance at the interfaces. It may be noted that the test circuits 30 may be placed along "saw" lines lying

between the integrated circuits, where they will be sawed apart, so as to avoid taking up space that might otherwise be occupied by additional integrated circuits. In order that each test circuit can include numerous interfaces, and the resistance across each interface can be individually measured, a considerable number of test tabs are required. It is desirable that the number of test tabs be minimal, so they occupy a minimum of space on the workpiece.

Fig. 3 illustrates a portion of a test circuit 30 of the present invention. The circuit includes numerous conductive tabs labeled T_1, T_2, etc., that are all formed in the upper layer 14. As also shown in Fig. 5, a conductive strip 32 is formed in the top layer 14 between tabs T_1 and T_2. Another conductive strip 34 is formed in the bottom layer 16 and joins the tabs T_3 and T_4 through interfaces. A third conductive strip 36 in the upper layer joins tabs T_5 and T_6. The conductive strips have conductive segments 40, 41, 42, 43, etc., which alternate between the upper and lower layers 14, 16 and which are interconnected by interface joints or interfaces 51, 52, 53, etc. These interfaces 51, 52, etc., are interfaces whose resistance or conductance can be measured by the method and apparatus of the present invention.

As indicated in Fig. 3, one way for measuring the interface resistance across the interface 51 is to pass a current "i" between tabs T_1 and T_4, so that current passes through the interface 51. While such a current is flowing, a voltmeter 62 is connected to tabs T_2 and T_3. Tab T_2 is connected to the upper layer at the interface 51, while tab T_3 is connected through an interface 64 and conductive segment 41 to the bottom layer at the interface 51. Since current is flowing between the top and bottom layers at the

interface 51 and the voltmeter is connected to the upper and lower layers at the interface, the voltage is proportional to the resistance across the interface. For example, if the current i is 100 microamperes and the voltage measured by the meter 62 is 10 microvolts, then the resistance across the interface 51 is 0.1 ohms and the conductance is 10 mho. While it is possible to repeat this procedure for each of the interfaces 51, 52, etc., applicant simplifies the procedure by passing a current through the entire chain of conductive segments and then measuring the voltage across the pairs of tabs connected to opposite sides of each interface. By applying current only once, applicant avoids the additional time required in each application of current, to wait for the current to settle down to a steady-state condition.

Fig. 4 illustrates a preferred test set-up for a test circuit 30 containing eleven interfaces whose resistance can be measured. The conductive segments 40, 41, 42, etc., are arranged along an imaginary line segment 81, with a pair of current tabs T_2, T_{23} at opposite ends, and with voltage tabs along opposite sides of the line segment. A current source 70 is applied between tabs T_2 and T_{23}, so the current flows between conductive strips 40, 41, 42, etc., located on the alternate layers, with the current flowing through the interfaces 51-60, etc., in passing between the layers. This establishes a predetermined current through each of the eleven interfaces 51-60.

While the current is flowing, a voltmeter 62 measures the voltage between a pair of tabs T_1 and T_4 which are in contact with opposite sides of the interface 51. After this voltage measurement, the voltmeter is connected between a next pair of tabs T_3 and T_6 to measure the voltage across interface 52. The voltage measurements continue across the tab pairs

T_5 and T_8, and T_7 and T_{10}, and so forth, until the tabs T_{21} and T_{24}. Thus, the test chain which enables the measurement of resistance or conductance across each of eleven interfaces, requires eleven pairs of tabs plus two tabs for the current source. Since the voltmeter 62 has a very high input impedence, its connection to the different pairs of tabs creates negligible transients, and the measurement of voltages across eleven pairs of tabs can be conducted rapidly. After the voltages across one test circuit 30 are completed, the test instrument can be moved to another test circuit on the wafer by lifting its twenty-four contacts off the tabs T_1-T_{24} of one test circuit and repositioning them on the test tabs of the next circuit.

It can be seen in Fig. 5 that the conductor portion, such as 72, which leads from the location where an interface 52 contacts the lower layer 16, extends from a side of the interface. Fig. 6 shows the general paths 73, 74, 75 of current flow between the conductive strip 41 and the interface conductor 22 which extends up to the upper layer. Much of the current i flows into the "front" 76 of the interface, while a significant portion flows into the sides 77, 78 of the interface. Very little current flows into the rear 79.

The lower layer 16 is generally of a material of much higher resistivity than the upper layer 14. Accordingly, a voltage measurement taken a small distance from the front 76 will include a voltage drop due to current flow through a length of the resistive strip 41. On the other hand, a voltage measurement taken a distance from the rear 79 where there is almost no current flow, will not include some of the voltage drop caused by currents 73-75 passing through the front and sides of the interface. Applicant takes a voltage

measurement from a side 77 (which leads to conductor portion 72 which extends to tab T_3), whose voltage is affected by much of the voltage drop through the interface but very little of the voltage drop along the current carrying strip 41. Having the conductor 72 extending from a location angled about 90° from the "front" location 76, with respect to an interface axis 81 normal to the lower layer and passing through the center of the interface, also enables the same voltage measurement whether from one side 77 or the other 78. In one test circuit, the conductors 41, 72 have a width W of three microns, while the interface has a width I of two microns.

Fig. 7 is a simplifed diagram of a test instrument 80. The instrument has twenty-four contacts labeled C_1-C_{24} which match the twenty-four tabs on a test circuit. A current source 70 is connected across the tabs C_2 and C_{23}. A group of relays 82, 84, 86, 88, etc., can be alternately closed to connect a pair of contacts such as C_1 and C_4 to an amplifier 90. The output of amplifier 90 can be delivered to a voltmeter 60, a memory 92, and a plotter 94. After each voltage measurement is taken, one of the relays 82 is opened, and the next relay such as 84 is closed. A control 96 turns on the current source 90, waits a short period of time for the current to settle, and then cycles the relays 82, etc., in sequence.

A wafer 10 (Fig. 1) may contain eighty-eight integrated circuits and eighty-eight test circuits 30, with each test circuit having perhaps eleven interfaces whose resistance is measureable. Thus, about one thousand interface resistance, or conductance, measurements can be made. Such a large number of measurements can be used to predict the probability of the integrated circuits failing because of excessive

resistance at one of their interfaces. Each integrated circuit may have perhaps 1,000 interfaces. As shown in Fig. 8, applicant establishes a predetermined minimum interface conductance level such as 1 mHo (1 ohms resistance), or even 0 mho, at which an integrated circuit is likely to fail. The conductance measurements at the eleven interfaces of each of the eighty-eight test circuits is then plotted on a normal probability graph of the type shown in Fig. 8.

A multiplicity of points 100 are established on the graph of Fig. 8, with each point having an ordinate R equal to the conductance measured in a measurement. Points of progressively lower conductance have an abscissa A that is progressively further from a minimum abscissa value 102. The points are spaced apart along the abscissa at probability intervals S about equal to one divided by the total number of points. Thus, if 1,000 measurements are taken, the first point 104 (of greatest conductance) will be at the abscissa value of 0.001, or 0.1%. The next point 106 will be at the abscissa value 0.2%, etc. When plotted on a normal probability graph of the type shown in Fig. 8, points further from the minimum abscissa level will be progressively closer together up to the probability of 50%; beyond 50% the points will be progressively further apart in the abscissa direction. An imaginary straight line 110 is fitted to the curve so that it is close to lying on all of the points (at least the majority of points of lowest conductivity). The line 110 can be extended to provide a useful measurement.

It can be seen in Fig. 8 that the point 112 representing the lowest conductance for all 1,000 measurements is still considerably above the lowest acceptable level which is one mho. (If the lowest acceptable level is much less than 10 mho, zero can be used as the lower level). The extension portion 114 of

the line 110 will intercept the minimum conductance level at a point 116 (representing five nines, or 99.999%). The probability of an interface having such a low conductance is indicated along the abscissa of the graph at the point 116, where the probability is 1 - 99.999% = 0.001%. In other words, the probability is 1/100,000 that an interface conductance will drop below the minimum permissible level for circuit operation. Where each integrated circuit has 1,000 interfaces, this indicates that only 1 circuit out of 100 is likely to have a failure. Fig. 8 shows another graph 120 for the test circuits on another wafer, where the average conductance is lower than in the graph 110. However, the line 120 connecting conductances arranged in order of conductance on the probability graph, shows a smaller slope of conductivity decrease with order of probability. The graph 120 intersects the minimum conductance level at the point 122, where the probability is 99.9999%, meaning that the probability of an interface failure is 1/1,000,000. The normal probability graphs of Fig. 8 can be plotted by hand or by a plotter as shown at 94 in Fig. 7.

Thus, the invention provides a test method and apparatus for facilitating the testing of interfaces between a pair of at least partially conductive layers on a workpiece which holds one or more integrated circuits. A test circuit includes a contact chain with multiple conductive segments alternating between the different layers and connected in series through interfaces connecting the beginning of a segment on one layer to the end of a segment on another layer. The chain includes a pair of end tabs at opposite ends of the chain of conductive segments, for passing a current through the chain, and pairs of tabs spaced along the chain and that are connected to the opposite sides of each interface along the chain. A test instrument

includes a current source for passing current between the end tabs and contacts for measuring the voltages across each pair of tabs that are connected to the opposite sides of each interface along the chain. The conductance measurements can be plotted on a normal probability graph with measurements of lower conductivity spaced progressively along the abscissa. A straight line drawn through the points will then pass through a minimum conductance level at a discernable probability level. One minus that probability equals the probability of failure of a single interface on the workpiece, such as in a test circuit or the integrated circuit.

Although particular embodiments of the invention have been described and illustrated herein, it is recognized that modifications and variations may readily occur to those skilled in the art, and consequently, it is intended that the claims be interpreted to cover such modifications and equivalents.

CROSS-CONTACT CHAIN

ABSTRACT OF THE DISCLOSURE

A system is provided for use with wafers that include multiple integrated circuits that include two conductive layers in contact at multiple interfaces. Contact chains are formed beside the integrated circuits, each contact chain formed of the same two layers as the circuits, in the form of conductive segments alternating between the upper and lower layers and with the ends of the segments connected in series through interfaces. A current source passes a current through the series-connected segments, by way of a pair of current tabs connected to opposite ends of the series of segments. While the current flows, voltage measurements are taken between each of a plurality of pairs of voltage tabs, the two tabs of each pair connected to opposite ends of an interface that lies along the series-connected segments. A plot of interface conductances on a normal probability chart, enables prediction of the yield of good integrated circuits from the wafer.

FIG. 1

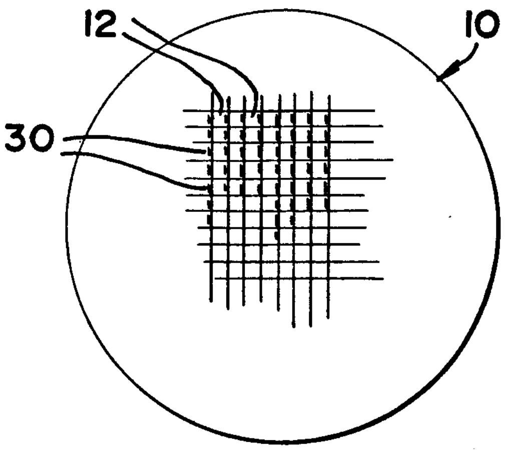


FIG. 2

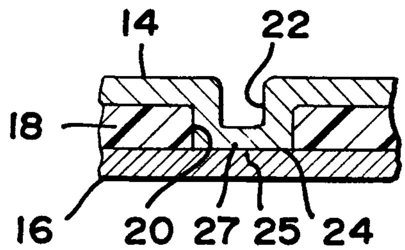


FIG. 3

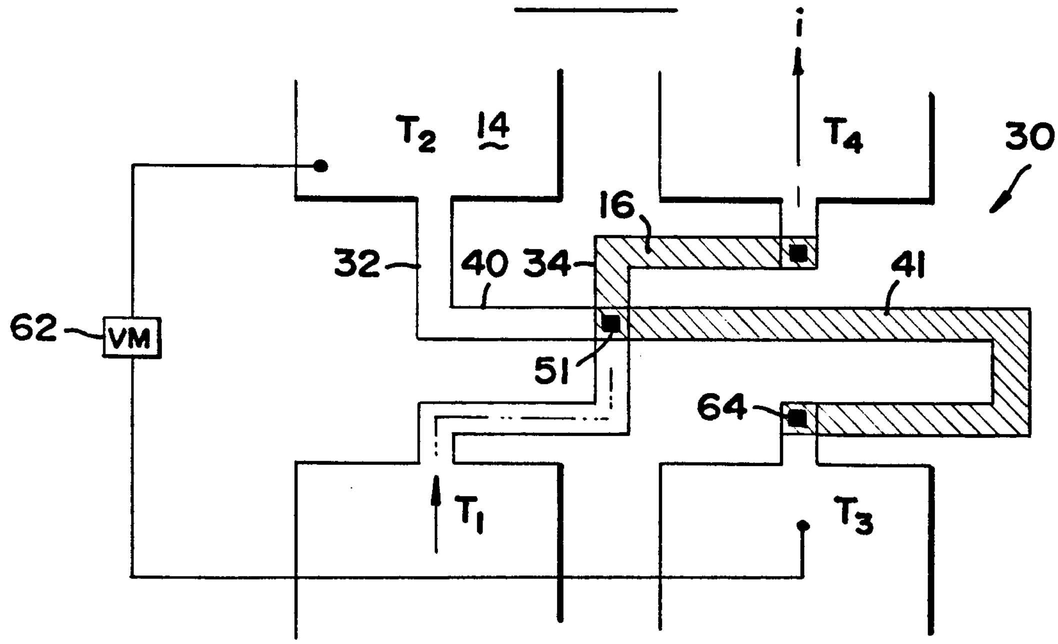


FIG. 4

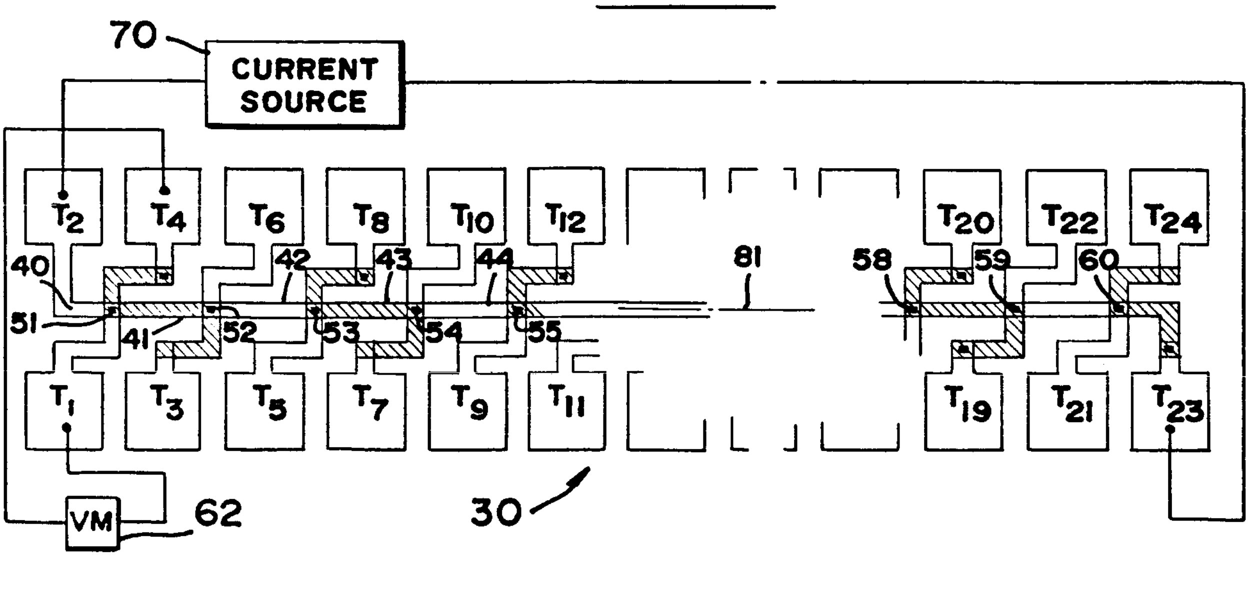


FIG. 5

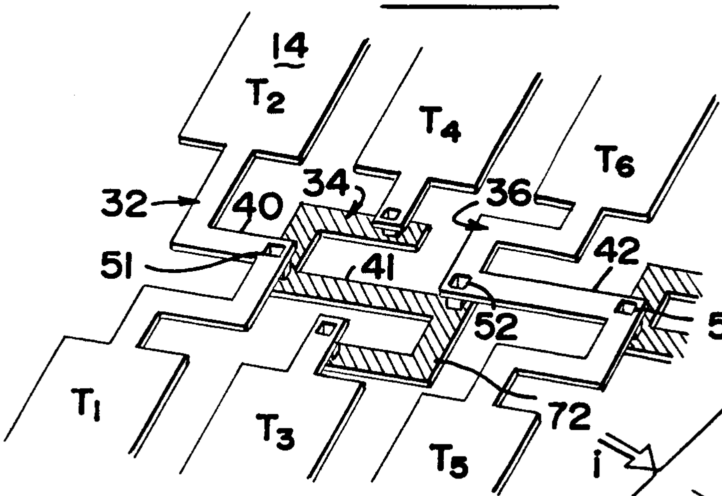
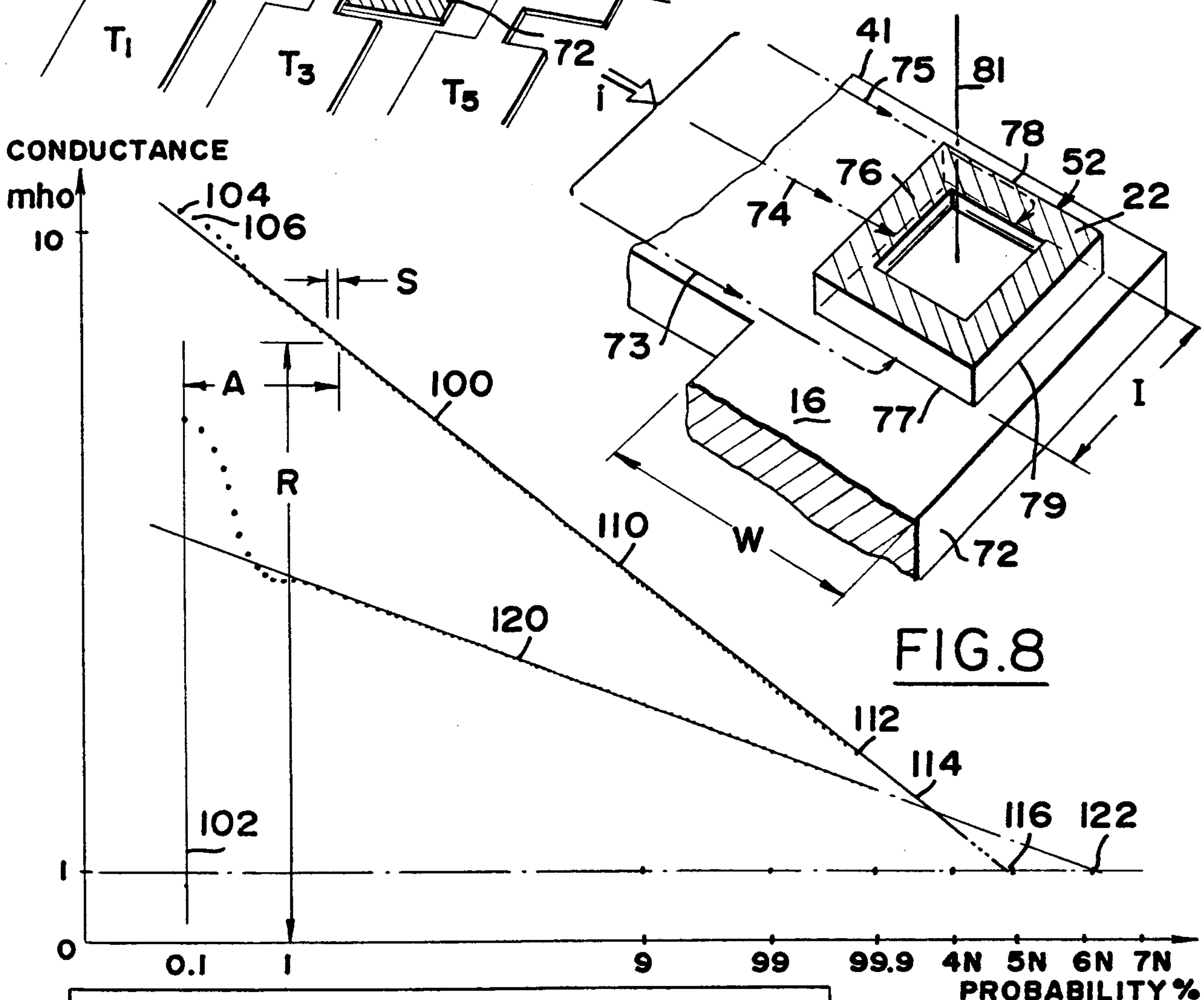


FIG. 6

FIG. 8



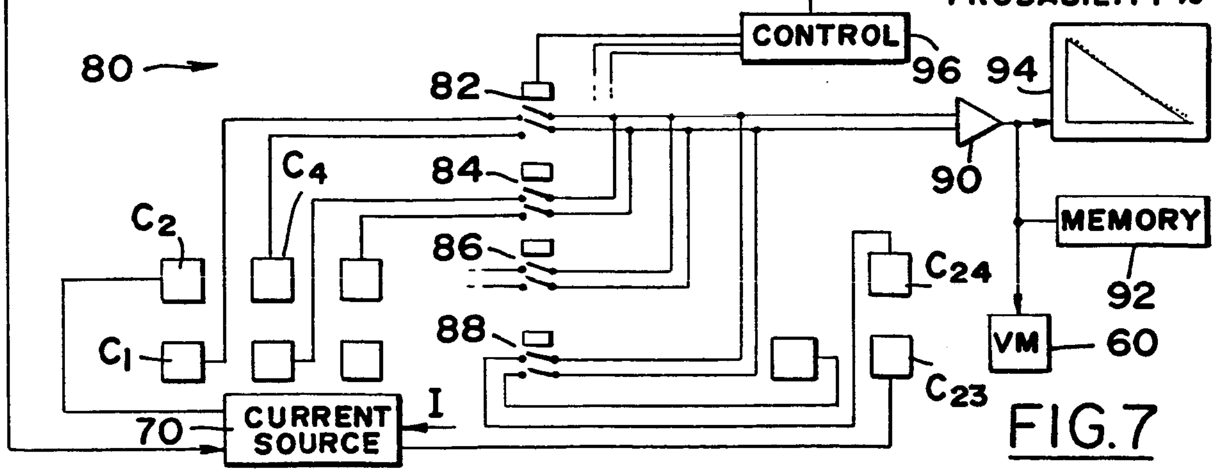


FIG. 7